

### **REMARKS**

Claims 1-22 remain in this application. Claims 1, 10, and 19 have been amended to put these claims into better form. The indication in the Office Action that claims 2-6, 11-18 and 20-25 are allowed is noted with appreciation as is the indication of allowability of claims 3, 4, 6, and 8. Claims 3, 4, and 8 have been written in independent form and thus, this group of claims is also allowable.

### **OBJECTION TO THE SPECIFICATION**

The title of the invention was objected to as not being descriptive. A proposed new title is presented above for the Examiner's approval.

### **REJECTIONS TO THE CLAIMS UNDER 35 U.S.C. § 102(b)**

Claims 1-2, 5, 7 and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by Dally and Poulton, Digital Systems Engineering, Figs. 12-50 and 12-51 ("Dally").

Claim 1 has been amended to indicate that the tails are connected "directly" to ground without any bias. As noted in the discussion of Dally in the specification, "this approach has its own problems... The textbook interpolator also requires a (noise prone) voltage bias to keep the tail current transistors saturated. Furthermore, common mode noise due to charge injection at the nodes between the tail and switching transistors is a problem which is described, but not solved, in the textbook version, when using equally weighted current sources." Thus, claim 1 which claims direct connections avoids one of the problems of the art, distinguishing thereover and is in condition for allowance, as are claims 2, 5, 7 and 9 which depend on claim 1..

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As noted above, claim 2, dependent on claim 1, is allowable as claim 1 is allowable. Furthermore, this claim is not anticipated by Dally. Dally only shows two phases. Note that claim 1 requires the coupling of each clock phase and its complement. Thus, the four phases of claim 2 require four pairs of transistors, not two as in the reference.

Claim 7 also has a feature not taught by the reference. Note the quote above: “Furthermore, common mode noise due to charge injection at the nodes between the tail and switching transistors is a problem which is described, but not solved, in the textbook version, when using equally weighted current sources.”

Finally in regard to, claim 9, Applicants note that they have been unable to identify the teaching in the reference, which the Examiner says is present regarding this point.

### **CONCLUSION**

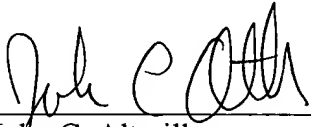
For all the above reasons, the Applicants respectfully submit that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

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The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,

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